



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/751,178	01/02/2004	Tae-Jung Lee	9898-325	3339

20575 7590 02/17/2006

MARGER JOHNSON & MCCOLLOM, P.C.  
210 SW MORRISON STREET, SUITE 400  
PORTLAND, OR 97204

EXAMINER

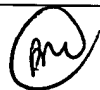
PHAM, LY D

ART UNIT PAPER NUMBER

2827

DATE MAILED: 02/17/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b> 10/751,178	<b>Applicant(s)</b> LEE ET AL. 	
	<b>Examiner</b> Ly D. Pham	<b>Art Unit</b> 2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) ☒ Responsive to communication(s) filed on 30 January 2006.
- 2a) ☒ This action is **FINAL**.      2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) ☒ Claim(s) 1-23 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 2-8 and 10-23 is/are allowed.
- 6) ☒ Claim(s) 1 and 9 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 02 January 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All    b) ☐ Some \*    c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

**FINAL ACTION**  
**DETAILED ACTION**

1. Applicant's Amendment filed January 30, 2006 has been entered. Claims 2 and 10 have been amended. Claims 24 – 33 have been canceled. Claims 1 – 23 are pending.

***Response to Arguments***

2. Applicant's arguments filed January 30, 2006 have been fully considered but they are not persuasive.

Contrary to applicant's remarks under the claim rejections under 102(e), the Korean priority filing date of the application does not suffice to overcome the rejection without the English translation of the certified priority document (see MPEP § 706.02(b), part E).

Therefore, the claims rejection remains as follow.

***Claim Rejections - 35 USC § 102***

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States

only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1 and 9 are rejected under 35 U.S.C. 102(e) as being anticipated by Kim et al. (US Pat 6,862,245 B2).

Regarding **claims 1 and 9**, Kim et al. disclose a dual port semiconductor memory cell (figs. 4 and 5), comprising:

a first CMOS inverter (I3) including a first NMOS transistor (N7), a first PMOS transistor (P4), and input port (coupled at node n3), and an output port (coupled at node n4);

a second CMOS inverter (I4) including a second NMOS transistor (N8), a second PMOS transistor (P5), an input port coupled to the output port of the first CMOS inverter and constitutes a first memory node together with the output port of the first CMOS inverter (at node n4), and an output port coupled to the input of the first CMOS inverter and constitutes a second memory node together with the input port of the first CMOS inverter (at node n3);

a third NMOS transistor (N5) having a gate coupled to a word line, a drain coupled to a bit line (BL), and a source coupled to the first memory node (node n3);

a fourth NMOS transistor (N6) having a gate coupled to the word line, a drain coupled to a complementary bit line (BLB), and a source coupled to the second memory node (node n4); and

a third PMOS transistor (P6) having a gate coupled to a scan address line (line SS from scan row decoder 14, fig. 5), a source coupled to the second memory node (node n4), and a drain coupled to a scan data-out line (line SL coupled to Sout, fig. 5);

wherein the plurality of memory cells are arranged in symmetry with respect to boundaries thereamong (fig. 5, memory cells MCs arranged symmetrically with respect to boundaries including surrounding memory cells).

5. The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

#### ***Allowable Subject Matter***

6. Claims 2 – 8, 10 – 16, and 17 – 23 are allowed.

7. The examiner's statement of reasons for allowance was provided in the previous Office Action mailed on November 01, 2005.

#### ***Conclusion***

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not

Art Unit: 2827

mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ly D. Pham whose telephone number is 571-272-1793. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ly D. Pham  
December 20, 2005

  
AMIR ZARABIAN  
SUPERVISORY PATENT EXAMINER  
TECHNOLOGY CENTER 2800